(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 February 2003 (27.02.2003)

PCT

(10) International Publication Number
WO 03/017541 A1

(51) International Patent Classification[7]: H04J 1/16, H04L 12/54, 12/56

(21) International Application Number: PCT/US02/25425

(22) International Filing Date: 9 August 2002 (09.08.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/930,804 15 August 2001 (15.08.2001) US

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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

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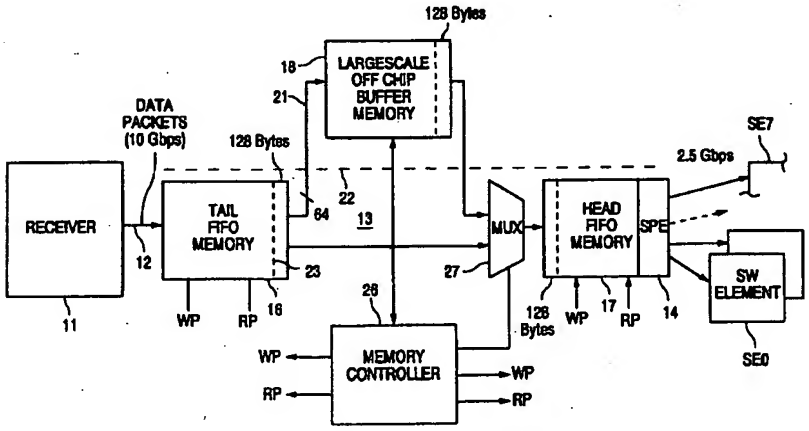
(54) Title: VARIABLE SIZE FIRST IN FIRST OUT (FIFO) MEMORY WITH HEAD AND TAIL CACHING



(57) Abstract: A variable size FIFO memory (13) is provided by the use of head (17) and tail (16) FIFO memories operating at a very high data rate and then an off chip buffer memory (18), for example, of a dynamic RAM type, which temporarily stores data packets when both head (17) and tail (16) FIFO memories are filled. Data blocks of each of the memories are the same size for efficient transfer of data. After a sudden data burst which causes memory overflow ceases, the head (17) and tail (16) FIFO memories return to the initial functions with the head memory directly receiving high speed data and transmitting it to various switching elements and the tails (16) FIFO memory stores temporary overflows of data from the head (17) FIFO memory.

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VARIABLE SIZE FIRST IN FIRST OUT (FIFO) MEMORY WITH HEAD AND TAIL CACHING

The present invention is structured to a variable size First In First Out (FIFO) memory with head and tail caching.

BACKGROUND OF THE INVENTION

Communications networks now require handling of data at very high serial data rates. For example, 10 gigabits per second (Gbps) is common. When it is required to process at these speeds, high speed data parallel connections are used to increase the effective bandwidth. This may be unsatisfactory because of the resultant decrease in bandwidth due to increased overhead requirements. There is a need for effective high speed switching apparatus and the associated hardware to support such a apparatus.

OBJECT AND SUMMARY OF INVENTION

It is therefore an object of the present invention to provide a variable size First In First Out (FIFO) memory.

In accordance with the above object, there is provided a variable size first in first out (FIFO) memory comprising a head FIFO memory for sequentially delivering data packets at a relatively slow rate to a plurality of switching elements whereby some latency occurs between data packets. A tail FIFO memory stores an overflow of the data packets from the head memory. Both the head and tail memories operate at a relatively high data rate equivalent to the data rate of incoming data packets. A large capacity buffer memory is provided having an effectively lower clock rate than the FIFO memories for temporarily storing data overflow from the tail memory whereby the FIFO memories in combination with the buffer memory form a variable size FIFO memory.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 is a block diagram of a memory embodying the present invention.

Fig. 2 is a diagrammatic portion of Fig. 1 illustrating its operation.

Fig. 3 is a flow chart of the operation of Fig. 1.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

As disclosed in a co-pending application entitled *High Speed Channels Using Multiple Parallel Lower Speed Channels* attorney docket 0679/13 switching of input data arriving at a relatively high data rate of, for example 10 Gbps, may be accomplished. As illustrated in Fig. 1 a plurality of switching elements SE0-SE7 which operate at a much lower data rate, for example 2.5 Gbps. By the use of a sequential or successive sprinkling technique for complete data packets a high data rate may be maintained. Data packets arrive from a receiver 11 which would have a communications processor coupled to it on line 12 at 10 Gbps and via the variable FIFO memory illustrated at 13, FIFO being First In First Out memory. Data packets are routed to a sequential sprinkler engine 14 and then distributed at the lower data rate to various switching elements. In general, a variable FIFO memory is required where a sudden burst of input data may occur which would temporarily overwhelm an individual FIFO memory without a large scale buffer memory (which it can be assumed has almost unlimited memory capacity since it is remote or off the same semiconductor chip as the high speed memory).

Fig. 2 illustrates where some latency may occur; in other words, there would not be a continuous serial transmission of the high speed data packets through to the switch elements. Thus the data packets 1, 2, 3 are indicated in a line of data being received. The first data packet is routed to the switching element 7. After this operation is started,. a short time later is indicated by the time lapse t_1 data packet two is distributed by the sprinkler engine; and then data packet three at a later time t_2. Some latency occurs which must be compensated for by some type of buffer apparatus.

This is provided by the overall variable FIFO memory which is a combination of a tail FIFO memory 16, a head FIFO memory 17 and the large scale off chip buffer memory 18. Variable blocks of data are formed by a receiver 11 and transferred through the tail FIFO memory to the head FIFO memory 17 until it is filled. Thus, the tail or FIFO 16 routes data to the head FIFO memory 17 which then distributes data packets to the various switching elements. If the head FIFO memory becomes full, the tail FIFO memory will start filling. The tail FIFO will buffer enough data to keep the head FIFO filled. If the tail FIFO fills due to a sudden burst, data is then written on the line of 21 to the large scale off chip memory 18. This data will be read from the large scale memory into the head FIFO when the head FIFO starts to empty.

From a practical standpoint to operate at the data rate of 10 Gbps, tail FIFO 16 and head FIFO 17 are located on a common semiconductor substrate or chip with the large scale buffer memory 18 being remotely located off chip. This is indicated by the dash line 22. When the tail FIFO memory becomes full then the large scale off chip buffer memory 18 is utilized. Uniform blocks of data are stored indicated by the dash line 23. For example, 128 bytes is transferred on the line 21 into the memory 18. This memory also includes a similar block size of 128 bytes. For example, line 21 may have a 64 bit width (meaning eight bytes) and thus, the data block of 128 bytes is transferred in 16 clock cycles (16x64=128 bytes). Optimization of the bus width in all of the FIFO and buffer memories provide, in effect, a 100 percent efficient transfer technique since for every clock cycle a maximum number of bits is transferred. However buffer memory 18 has a lower clock rate and therefore wider bus. In the present application this could be two read and two write cycles. The various write pointers and read pointers (WP and RP) are so indicated on the various memories and the overall control is accomplished by the memory controller 26. A multiplexer 27 connected to memory controller 26 provides for control of the various data routings. When a sudden burst of data packets ceases, the FIFO memory can then return to its ordinary mode of operation where the head FIFO memory 17 contains all of the inputted data packets as delivered by the tail FIFO memory. Of course, this doesn't occur until the large scale off chip buffer memory 18 is unloaded.

The foregoing operation is shown in a flow chart of Fig. 3. In step 41 the head FIFO memory is filled, and in step 42 if the head FIFO overflows, the tail FIFO memory is filled. Then in step 43 again when the tail FIFO is filled, data is stored in the buffer memory until the head FIFO begins to empty. In general, memory controller 26 monitors the FIFO depth and determines if a block of data needs to be stored to off chip memory. It also keeps track of how many blocks are written. As the FIFO memories empty, the memory controller is responsible for arbitrating and retrieving any stored blocks of data.

The larger external buffer memory 18 can be provisioned, using one of many allocation schemes, to support multiple head and tail FIFOs in the same manner as described.

Thus a variable FIFO memory with head and tail caching has been provided.

CLAIMS:

1. A variable size first in first out (FIFO) memory comprising:

a head FIFO memory for sequentially delivering data packets at a relatively slow rate to a plurality of switching elements whereby some latency occurs between data packets:

a tail FIFO memory for storing an overflow of said data packets from said head memory; both said head and tail memories operating at a relatively high data rate equivalent to the rate of incoming data packets;

a large capacity buffer memory having an effectively lower clock rate than said FIFO memories for temporarily storing data overflow from said tail memory whereby said FIFO memories in combination with said buffer memory for a variable size FIFO memory.

2. A memory as in claim 1 where said head and tail memories have data blocks of a predetermined and same size and said buffer memory has the same size data block whereby high efficiency data transfer between memories is obtained.

3. A memory as in claim 1 where FIFO memories reside on a common semiconductor substrate and said buffer memory is remote.

4. A memory as in Claim 1 where said buffer memory has a wider bus than said head and tail FIFO memories.

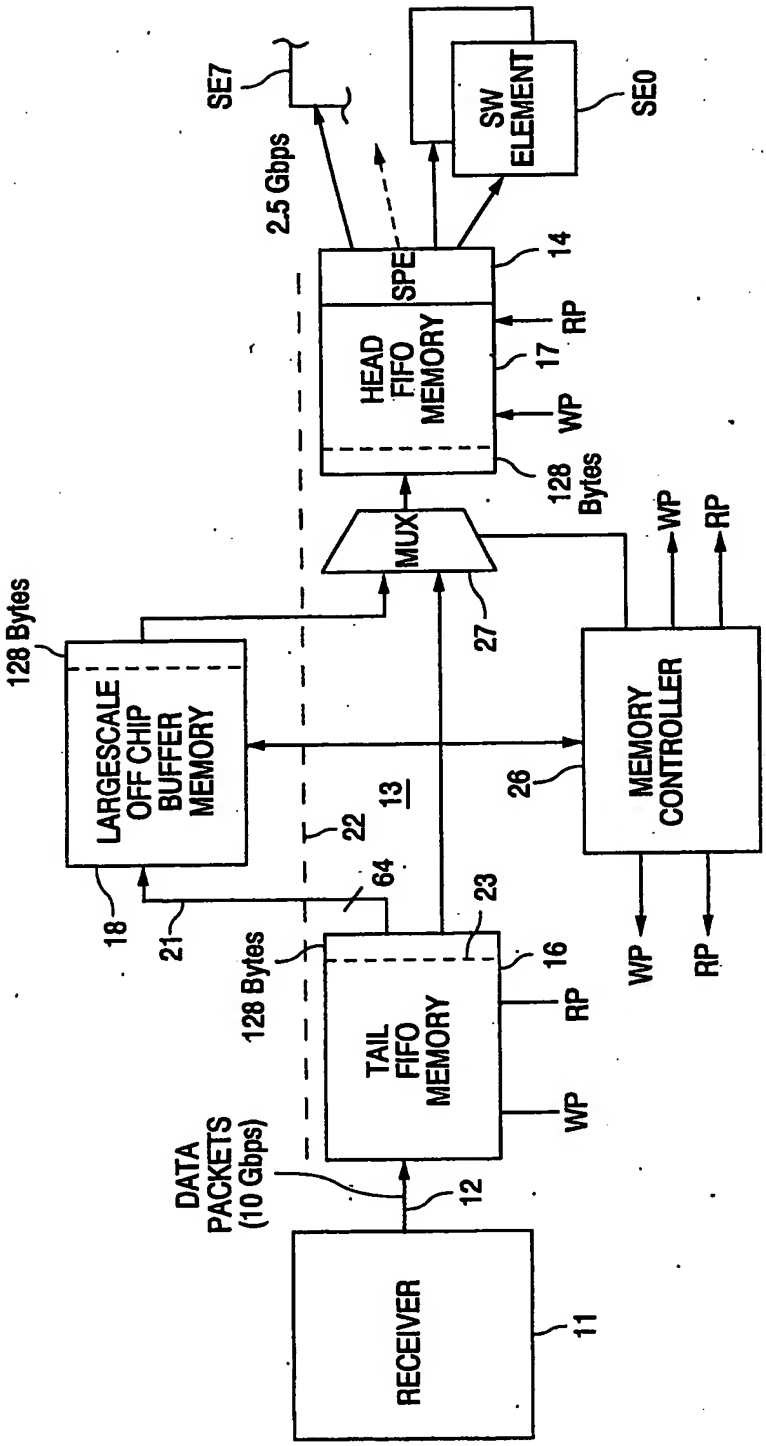
SE7
SW ELEMENT
SE0
2.5 Gbps
SPE
14
HEAD FIFO MEMORY
RP
17
WP
128 Bytes
MUX
WP
RP
27
128 Bytes
LARGESCALE OFF CHIP BUFFER MEMORY
13
22
64
23
26
MEMORY CONTROLLER
18
21
128 Bytes
16
RP
WP
TAIL FIFO MEMORY
DATA PACKETS (10 Gbps)
12
RECEIVER
11

FIG. 1

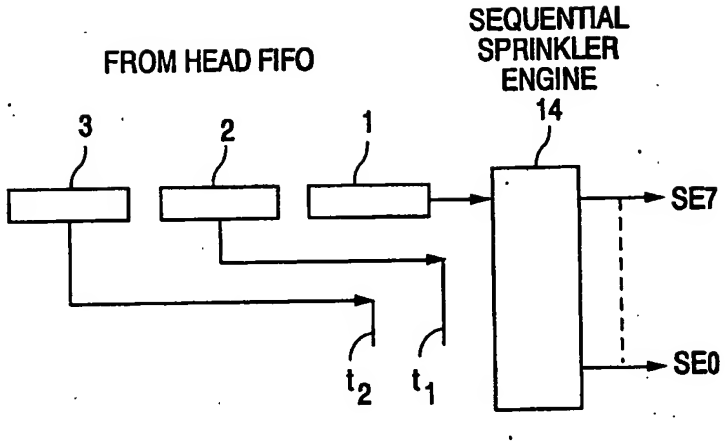
FROM HEAD FIFO
SEQUENTIAL SPRINKLER ENGINE
14
3
2
1
SE7
SE0
t_2
t_1

FIG. 2

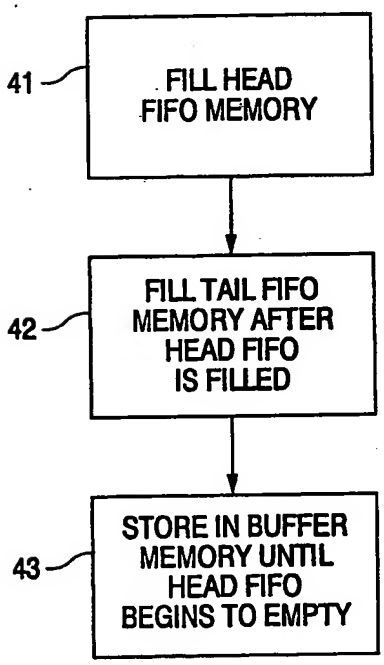
41
FILL HEAD FIFO MEMORY
42
FILL TAIL FIFO MEMORY AFTER HEAD FIFO IS FILLED
43
STORE IN BUFFER MEMORY UNTIL HEAD FIFO BEGINS TO EMPTY

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/25425

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H04J 1/16; H04L 12/54, 12/56
US CL : 370/231, 232, 253, 395.7, 412, 429
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 370/231, 232, 253, 395.7, 412, 429

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST Database

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6,122,674 A (OLNOWICH) 19 September 2000 (19.09.2000), see the entire document.	1-4
Y	US 5,982,749 A (DANIEL et al) 09 Novenmber 1999 (09.11.1999), see the entire document.	1-4
A	US 4,394,725 A (BIENVENU et al) 19 July 1983 (19.07.1983), see the entire document.	1-4

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Date of the actual completion of the international search	Date of mailing of the international search report
26 September 2002 (26.09.2002)	19 DEC 2002
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Toan Nguyen Telephone No. 703-305-9600

Form PCT/ISA/210 (second sheet) (July 1998)

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